REMARKS

In light of the following remarks, reconsideration of the present application is respectfully requested. Claims 1-26 are pending in this application. Claims 1, 10, 17 and 22 are independent claims. No new matter has been added.

Allowable Subject Matter

As indicated by the Examiner, claims 5-9, 12-16, 20-21 and 24 define allowable subject matter. However, as all claims are believed to be allowable, these claims have merely been maintained in their current form.

Rejections Under 35 U.S.C. § 103

1. Claims 1-4, 17-19, 22, 23 and 26 stand rejected under 35 U.S.C. §103(a) as being obvious over Morikawa et al. (US 2001/0032297) in view of Arimilli et al. (US 2002/0087815). Applicant respectfully traverses this rejection for the reasons detailed below.[1]

Claim 1

Claim 1 requires, inter alia, "a first cache memory for enabling a running flag signal in response to a given interrupt signal ... and for disabling the running flag signal." This feature is not disclosed or suggested

[1] To be thorough, further expedite prosecution, and for the sake of clarity, Applicants provide discussions throughout this Request for Reconsideration of each of the references separately. However, Applicants are not attacking these references individually, but arguing that the references, even taken in combination, fail to render the claimed invention obvious because all features are not found in the prior art.

in Morikawa et al., Arimilli et al. or a combination of the two (assuming *arguendo* that they can be combined, which Applicant does not admit).

Morikawa et al. discloses a cache memory apparatus including a processor 1, a lower-level memory 9 and a cache apparatus 5 having a naked cache 6 and a cache-miss cache memory 7. A target flag 19 holds storage destination cache information. During a prefetch instruction that produces a cache-miss, processor 1 sets target flag 19 to "0" via a control signal line 17 and orders the data to be stored in naked cache memory 6. If it is not a prefetch instruction and there has been a cache-miss in both naked cache memory 6 and cache-miss cache memory 7, processor 1 sets target flag 19 to "1" via control signal line 17 and orders the data to be stored in the cache-miss cache memory 7.

The Examiner admits that Morikawa et al. does not teach a cache memory enabling a running flag signal. Additionally, the Examiner relies upon the setting of target flag 19 to "1" of Morikawa et al. to teach "disabling the running flag signal," of claim 1. But, in Morikawa et al., the processor 1 sets the target flag 19 to "1." Processor 1 is not a first cache memory. Accordingly, Morikawa et al. does not disclose "a first cache memory ... disabling the running flag signal," as required by claim 1.

Arimilli et al. discloses a microprocessor reservation mechanism having a processing core 42 and a cache 44 including three cache slices 50a, 50b and 50c. Each of cache slices 50a, 50b and 50c has a separate reservation unit, that is, a reservation flag and an address field for the reservation field. When core 42 issues a load with reserve (larx) request, the

request is broadcasted to all of cache slices 50a, 50b and 50c. The larx broadcast initially clears each reservation flag. If the broadcast arrives at the target cache slice coincident with the actual operation, control logic at the corresponding reservation unit overrides the larx broadcast, and allows the corresponding reservation flag to be set. The reservation flag and the target cache slice can be reset in response to a conditional store command, or in response to a snooping operation from an adjacent processing unit. The reservation flag will also be reset if another load with reserve operation, directed to a different cache slice results in the issuance of another broadcast. See paragraphs [0033]-[0035].

The Examiner relies upon the above-described "reservation means" (recited in claim 9, page 5 of Arimilli et al.) that sets a "reservation flag" to teach "a first cache memory enabling a running flag signal," as required by claim 1. However, the "reservation flag" is not a running flag signal. The reservation flag indicates an operation may write to the block for which the reservation exists. See paragraph [0011]. Furthermore, once the block for which the reservation exists is written to, the flag is reset. See paragraph [0012]. Accordingly, the "reservation means" that sets a "reservation flag" is not a first cache memory enabling a running flag signal.

Therefore, even assuming *arguendo* that Morikawa et al. and Arimilli et al. can be combined (which Applicant does not admit), the combination does not disclose "a first cache memory for enabling a running flag signal in response to a given interrupt signal ... and for disabling the running flag

signal." Consequently, claim 1 and its dependent claims are patentable over Morikawa et al. and Arimilli et al.

Claims 17 and 22 and their respective dependent claims are patentable for at least the reasons set forth above.

For at least the foregoing reasons, Applicant respectfully requests that the rejections of these claims be withdrawn.

2. Claims 10, 11, 13 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Morikawa et al. in view of Arimilli et al. and Chiu et al. (US 6,505,253). Applicant respectfully traverses this rejection for the reasons detailed below.

Claim 10

The Examiner correctly acknowledges that the features of claim 10 are absent from Morikawa et al. in view of Arimilli et al., but alleges that these features are taught by Chiu et al., thereby rendering claim 10 obvious to one of ordinary skill at the time of the invention. Even assuming *arguendo* that the features of claim 10 are taught by Chiu et al. (which Applicants do not admit) and that Chiu et al. could be properly combined with Morikawa et al. and Arimilli et al. (which Applicants do not admit), Morikawa et al., Arimilli et al. and Chiu et al. are still deficient with respect to the above-described features of claim 1. Thus, even in combination, Morikawa et al., Arimilli et al. and Chiu et al. fails to render claim 10, and its dependent claims, obvious.

Therefore, Applicant respectfully requests that the Examiner withdraw this rejection.

CONCLUSION

In view of the above remarks and amendments, Applicant respectfully submits that each of the rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By _____

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